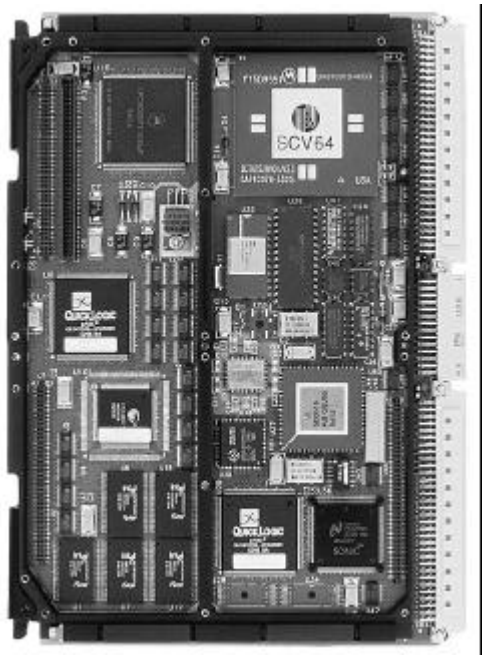
SVME/DMV-177

PowerPC 603e Single Board Computer with MAXPack Interface

Features

- *PowerPCÔ 603e RISC CPU at 100MHz**
- *Up to 64M bytes DRAM with EDAC*
- *8Mbytes 64-bit Flash™ EPROM*
- *2Mbytes low cost boot Flash™ EPROM*
- *256kbyte EEPROM*
- *512 byte serial EEPROM*
- *Support for one MAXPack module, providing flexible I/O expansion*
- *On-board Ethernet with AUI interface*
- *On-board SCSI-2 interface*
- *Four 16-bit counter/timers*
- *Two EIA-422 and two EIA-423 serial channels*
- *Real-Time Clock (RTC)*
- *Tick and watchdog timers*
- *Advanced VME Interface Chip (SCV64)*
  - *A32:D32 VMEbus interface with A64:D64 MBLT support per ANSI/VITA 1-1994, VME64*
  - *Location monitor with FIFO buffer*
  - *Bus Isolation mode (BI-mode®)*
  - *Auto-ID and Auto-SYSCON*
  - *System controller functions*
- *Built-In-Test (BIT)*
  - *95% fault coverage*
- *Front-panel JTAG/COP™ Interface*
- *Foundation firmware including:*
  - *Debug monitor*
  - *Diagnostics*
  - *Card Support Services*
  - *Execution Sequencer*
  - *Non Volatile Memory Programmer*
- *Conduction cooled per IEEE 1101.2 (0.80-inch pitch) for MIL-E-5400/4158, and MIL-STD-2036 applications*
- *Optional levels of ruggedization*

** Contact DY 4 for latest CPU speed availability*



Description

The latest in the growing line of DY 4 PowerPC-based SBC products, the SVME/DMV-177 Single Board Computer combines a high-performance 100 MHz PowerPC 603e RISC processor with up to 64M bytes of DRAM, with Error Detection and Correction, together with up to 10M bytes of Flash EPROM on a single-slot assembly. Numerous sub-system functions including Ethernet, SCSI-2, and four serial ports are included on-board. Programmable low-power modes provide power savings to match system requirements. The card is equipped with DY 4's MAXPack interface, an open standard mezzanine module approach which allows system designers to increase the assembly's functionality by incorporating one of several standard MAXPack modules, or developing their own custom module.

The SVME/DMV-177 provides a highly integrated approach in a single-slot solution with raw processing performance, industry standard I/O, and User-specific I/O which traditionally required multiple boards. Figure 1 shows a block diagram of the SVME/DMV-177 SBC. The SVME/DMV-177's design features address mission-critical demands of military and aerospace systems integrators with increased computing performance, self-test coverage and functional density.

The card supports DY 4 Systems' common features including an VME64 VMEbus interface, Built-In-Test (BIT), BI-mode, location monitor, and Auto ID. These features bring benefits in performance, logistics and maintenance.

DY 4's industry-standard SCV64 chip implements all VMEbus interface functions with software-programmable features. It combines low-latency access to the VMEbus with high sustained throughputs. Built-In-Test (BIT) hardware features verify all operational circuits on the module. Bus Isolation mode (BI-mode®) increases ease of testing and system fault location.

The location monitor supports efficient interprocessor messaging, to minimize overhead in real-time software. Auto-ID allows boards to be self-configuring, based on slot

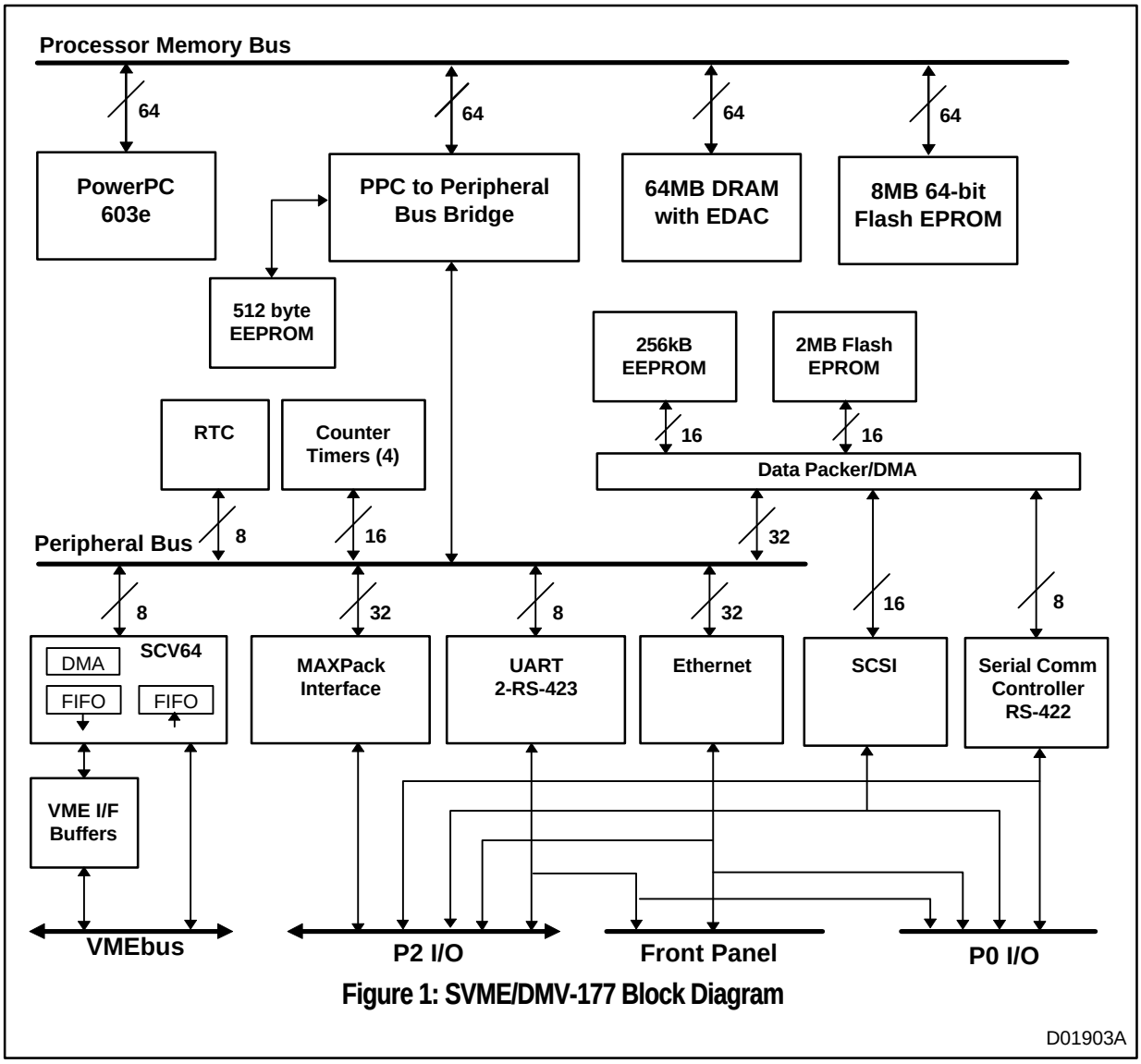


Figure 1: SVME/DMV-177 Block Diagram

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location.

These features allow users to:

- build high-performance multi-processor systems
- detect and isolate faults during operation
- minimize field maintenance and sparing logistics.

All versions of the SVME/DMV-177 are functionally identical with the exception that Ethernet is omitted on level 200/300 product and not all memory configurations are available. SVME air-cooled versions are available in DY 4 ruggedization levels 000, 100 and 200.

The conduction-cooled DMV version is designed for airborne, land-mobile, and naval military applications where circuit cards could be sealed in a chassis to prevent moisture, salt-fog, sand, and dust contamination. DY 4 Systems' conduction-cooled products are designed for severe environmental conditions defined by MIL-E-4158, MIL-E-5400, and MIL-STD-2036. A Copper Core Cooled PWB conducts heat away from the electronics. An additional stiffening frame improves heat dissipation and vibration resistance. Standard wedgelock fasteners give a reliable thermal connection to the chassis. DMV conduction-cooled versions are available in DY 4 ruggedization levels 100 and 200.

CPU

The PowerPC 603e CPU is a high-performance, low-power 64-bit RISC microprocessor developed by Apple, IBM, and Motorola for the growing commercial desktop industry. The PowerPC 603e on the SVME/DMV-177 runs at 100 MHz on-chip and offers estimated benchmarks 120 SPECint92 and 105 SPECfp92 (with internal cache on).

Containing separate instruction and data caches, 64-bit data paths, and software programmable power-saving modes, the PowerPC 603e CPU integrates the following:

- Superscalar multiple instruction-per-cycle architecture
- 32- and 64-bit Floating Point Processor (FPP)
- 5 separate parallel instruction units
- 16K byte instruction cache
- 16K byte data cache
- 32- or 64-bit data bus
- 3.3V design with 4 power-down modes

Memory

SVME/DMV-177 SBC DRAM is located on a memory mezzanine module. Memory consists of high performance DRAM which can be factory configured as either 8, 16, 32 or 64 Mbytes. The memory is accessible from the on-board CPU, the VMEbus, the SCSI and Ethernet chips, and the MAXPack interface. The memory interface design supports PowerPC 603e burst mode accesses, providing 5.3.3.3 burst performance with EDAC turned off (6.4.4.4. with EDAC on).

The SVME/DMV-177 supports of a mix of Flash EPROM and EEPROM devices for over 10M bytes of on-board non-volatile memory storage. On-board non-volatile memory consists of:

- 64-bit wide Application Flash
- 16-bit wide low-cost boot Flash
- 16-bit wide Application EEPROM

Application Flash provides the capability of high performance program execution directly from EPROM. A low-cost 2M bytes Flash memory boot site and 256K bytes of EEPROM are also available.

Non-volatile memory is not VME-visible and is re-programmable in-circuit via DY 4's integrated Non-Volatile Memory Programmer (NVMP) or FlashProg utility over the VMEbus, the serial port, or the Ethernet port.

The SVME/DMV-177 SBC has a 512 byte serial EEPROM for storing configuration data.

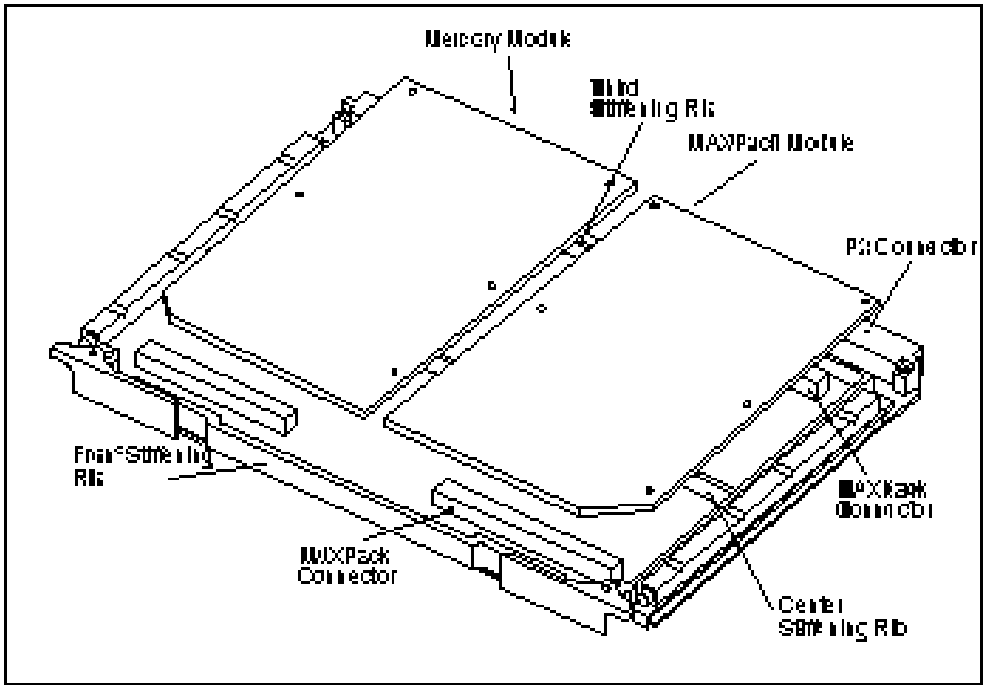

Figure 2: Base Board with MAXPack (Shown with memory module)

MAXPack Interface

The SVME/DMV-177 SBC is equipped with a MAXPack mezzanine module interface. MAXPacks may be used to add a variety of I/O functions to the base board. MAXPack modules conform to an open specification that defines the electrical and mechanical interface, thus permitting customers to design special function modules. Future generations of DY 4's RISC-based SBCs will carry the same MAXPacks, thus providing a performance growth path that preserves the software invested in the MAXPack.

The MAXPack mechanical design is suited to high shock and vibration environments. The modules are rigidly mounted to the base board along three stiffening ribs and also along a rib parallel to the card edge. This arrangement is structurally rigid, and it provides a low-resistance thermal path for heat removal.

All I/O connections of the MAXPack module are brought out on the P2 connector of the SVME/DMV-177 SBC. Figure 2 shows a conceptual view of the assembly with the SVME/DMV-177 memory module.

Programmable Power Modes

The SVME/DMV-177 has several User-programmable power saving modes which lower the power consumption under certain conditions, resulting in a very low power full-featured military product. Under operating system control, full-power operation results in 19 W consumption (typical) while Idle Mode results in 14 W consumption (typical) for an SBC configured with the maximum amount of memory and sub-system options.

VME Interface

The VMEbus interface of the SVME/DMV-177 SBC is implemented with DY 4's industry-standard Single Chip VMEbus Interface, (SCV64), which provides all the elements of a complete VMEbus interface. The philosophy of the SCV64 design is to provide programmable features that eliminate the need for jumpers, thereby simplifying logistics

and reducing sparing requirements. The SCV64 incorporates the following features:

- System Controller
- Master/slave A64:D64 interface
- Tx and Rx FIFO's to decouple bus operations
- Location monitor with FIFO message queue
- Interrupter, interrupt handler
- Extensive Built-in-Test support

The SCV64 provides all VMEbus system controller and interrupt functions. It allows for full programmability of requester modes and levels, arbiter modes, bus timers, interrupt levels and vectors. The SCV64 also features extensive BIT features and BI-mode®.

A primary function of the SCV64 is to allow the CPU to access the VMEbus, and to allow the VMEbus to access on-board memory. The SCV64 contains transmit and receive FIFO's which are used to implement a store-and-forward technique of bus decoupling. SCV64-equipped CPUs can write to VMEbus locations without incurring a delay while the VMEbus is requested, arbitrated, and the bus grant received. For moving large blocks of data between on-board memory and the VMEbus, the SCV64 provides an integral DMAC. Bi-directional transfers can be configured to occur in discrete, block, or multiplexed block (D64) mode. Real throughput of up to 60 Mbytes/sec may be achieved.

To support inter-processor message passing, the SCV64 provides a location monitor (LM) with a built-in FIFO message queue. A write access to the LM results in capture of the data, and causes an interrupt to the CPU. The message queue is organized as a 32-bit wide FIFO with 31 entries.

Ethernet Interface

An on-board IEEE 802.3 compliant Ethernet interface is provided to eliminate the requirement for a separate Ethernet board elsewhere in the system. Available in both SVME and DMV versions at level 000 and 100, this LAN interface may be used for card-level download and debug or may be incorporated into a deployed system for a 10 Mbit/s communication port. A fuse-protected 3-pair transformer-coupled front-panel AUI port is available on the SVME versions. DMV versions use the P0 of P2 backplane connectors. The LAN interface is implemented with a National Semiconductor 83932B SONIC™ device.

SCSI-2 Interface

The SVME/DMV-177 provides a single-ended, 8-bit wide SCSI-2 compliant interface. Using the QLOGIC Fas 216 and a high speed DMA controller, peak SCSI bus speeds of 5 Mbytes/second (asynchronous) or 10 Mbytes/second (synchronous) are supported. The DMA controller acts independently of the PowerPC to transfer data between the local memory and the SCSI controller IC. This allows the PowerPC 603e and the other on-board I/O processors to continue to handle processing tasks while data is being transferred to the SCSI bus. The DMA data packer assembles bytes into 32-bit words, resulting in more efficient usage of the memory bandwidth.

Serial Interfaces

The SVME/DMV-177 provides two asynchronous/synchronous EIA-422 serial channels and two asynchronous EIA-423 serial channels. The EIA-422 channels support asynchronous data rates of from 75 to 38.4K bps. In synchronous mode the EIA-422 channels support data rates up to 613K bps. By using the DMA support one channel can be operated at up to 1M bps. Both EIA-422 channels support handshaking (1 in/1 out). The data rates of the EIA-423 channels are programmable from 75 to 38.4K bps. Interrupts are also programmable under software control. The EIA-423 serial channels are available at the P0 connector and at the front panel connector on the SVME versions or they may be optionally routed to the P2 connectors.The two EIA-422 serial channels are normally available on the P0 connector but may be optionally routed to the P2 connector.

Real-Time Clock (RTC)

The SVME/DMV-177 is equipped with a Harris 7170 RTC chip to provide for time-of-day calculations. It contains registers for year, month, day, day-of-week, and seconds through to hundredths of seconds, and interrupt controls. Leap-year and days per month are automatically updated. The RTC is capable of periodic or alarm/wake-up interrupts to the CPU.

The RTC may be powered from the +5V STDBY line, therefore it can continue to maintain the time during loss of main power.

Timers

There is an on-board tick timer which can be programmed to interrupt the CPU at regular intervals. Hardware watchdog timers provide a fail indication or reset the CPU if an execution failure is detected. Watchdog Timer intervals may be either 100 ms or 2 s.

There are four additional 16-bit timers available to the user, providing a basic interrupt on terminal count. A programmable interrupt output is provided, and three of timers are cascadable.

System Status Signals/Switches

The SVME/DMV-177 SBC provides a status signal on the P2 connector. This signal asserts in the event of a card failure, and corresponds to the front panel indicator red LED, permitting a test connector to be incorporated in a sealed conduction-cooled chassis. A User programmable status green LED is included. A card reset switch is mounted on the front panel in SVME versions only (card reset is also available via P0).

JTAG/COPÔ Interface

The SVME/DMV -177 implements the 603e's JTAG and Common On-chip Processor (COP) functions via a front panel 16-pin connector (SVME only) and P0. The JTAG boundary scan features can be used for board-level testing while the COP features will be used mainly for chip/code debug using a work station tool such as the IBM RISCWatch ® 603e development station. The JTAG features and interface are compliant with IEEE 1149.1.

Available MAXPacks

The capabilities of the SVME/DMV-177 SBC can be enhanced by adding a MAXPack module. MAXPack modules are available in all standard DY 4 ruggedization levels, for use with both air-cooled and conduction-cooled base boards. MAXPacks that are available or currently in development include:

- MAX-651 Single 1553B.
- MAX-654 Dual 1553B Controller, provides two redundant 1553B interfaces. Support for 1553A, and 1553B Notice 2. Modes include BC, RT and BM
- MAX-657 Single 1553B, Utility Bus and voice record and playback.

Foundation Firmware

The SVME/DMV-177 SBC is supplied with a foundation firmware package. Refer to document number 804168 *Foundation Firmware* for more information about:

- General Purpose Monitor (GPM) - provides comprehensive monitoring and debug functions for the system integrator (refer to General Purpose Monitor
- Card Level Diagnostics (CLD) - provides diagnostic routines which perform a self-test function in conjunction with the Built-In-Test equipment
- Card Support Services (CSS) - provides a common software interface to the hardware features on the card, device independent I/O functions generic exception processing routines, and Auto-ID services
- Execution Sequencer (ES) - controls the invocation order of the Software Configuration Items on the card
- Non Volatile Memory Programmer (NVMP) - provides for in-circuit programming of Flash memory.

Built-in Test

Incorporated in Foundation Firmware via Card Level Diagnostics, DY 4's BIT is extensive and full-featured. A 95% confidence level is provided, as well as the storage of results of BIT in RAM. A small portion of RAM is reserved for routine BIT storage in form of a Diagnostics Results Table (DRT), which is accessible via VMEbus, serial port, or via the MAXPack interface while an application is running. Given proper Power Down notification, the DRT can be written to ROM and read later (such as at depot level).

Software

A variety of real-time operating systems, application programs, and software tools are available for the SVME/DMV-177. Planned operating systems include:

- VxWorks
- VADSCross
- VADSworks
- LynxOS

Custom Variants

Custom variants can be provided if the one of our standard variants is not suitable. Contact your local sales representative for cost and availability. SVME/DMV-177 options and accessories include:

- DRAM capacity from 8 Mbytes to 64 Mbytes
- Non-volatile memory of EEPROM or FLASH
- Depopulated SCSI and Ethernet
- Factory installation of MAXPack modules
- Custom MAXPacks for User-defined I/O.
- P2 I/O cable for development system use
- FlashProg Flash EPROM programming utility
- VxWorks Board Support Package

SVME -177 cards are available in ruggedization levels 000 to 200. DMV-177 cards are available in levels 100, 200 and 300.

Other Single Board Computers from DY 4

DY 4 produces a full line of both CISC and RISC single board computers with a variety options.

- **SVME/DMV-162** SBC with 68040 CPU up to 8MB SRAM and 8MB Flash EEPROM
- **SVME/DMV-163** SBC with 68040 CPU up to 64MB DRAM and 4MB Flash EEPROM
- **SVME/DMV-166** SBC with 68040 CPU up to 8MB SRAM and 8MB Flash EEPROM
- **SVME/DMV-176** SBC with PowerPC 603e RISC CPU, up to 12MB SRAM and 10MB Flash EEPROM

For more information call your local sales representative.

Table 3
Specifications

ENVIRONMENTAL SPECIFICATIONS		
Temperature	**(Level 0)**	
Operating	0°C to 50°C	MIL-STD-810
Storage	-40°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Level 1)**	
Operating	-40°C to 71°C	MIL-STD-810
Storage	-55°C to 85°C	Methods 501.3 & 502.3
Temperature	**(Levels 2, 3)**	
†Operating	-55°C to 85°C	MIL-STD-810
Storage	-62°C to 125°C	Methods 501.3 & 502.3
Humidity (DMV CCA and SVME CCA - Levels 1,3)		
Operating	0 to 95% non-condensing	MIL-STD-810
Non-Operating	0 to 100% condensing	Method 507.3
Vibration (DMV)		
Sine	10g at 15 to 2,000 Hz	MIL-STD-810
Random	$0.1g^2/Hz$	Method 514.4
Shock (DMV)	40g/11ms half sine	MIL-STD-810 Method 516.4, Proc 1
Altitude (DMV L200)	30,500m (100,000 ft)	MIL-STD-810 Method 500.3

DIMENSIONS	**DMV CCA**	**SVME CCA**
Height	233.4 mm (9.2 in.)	233.4 mm (9.2 in.)
Depth	160 mm (6.3 in.)	160 mm (6.3 in.)
Thickness	20.0 mm (0.8 in.)	20.0 mm (0.8 in.)
Weight	<900g (<2 lb)	<570g (<1.28 lb)

POWER REQUIREMENTS	**(Base card, fully populated)**	
+5v (+5%, -2.5%)	4.5 A (maximum)	2 A(typical)
+5v STDBY (operating)	tbd A (maximum)	tbd A (typical)
+5v STDBY (standby)	tbd mA (maximum)	tbd mA (typical)
+12v (+5%, -3.0%)	18 mA (maximum)	11 mA (typical)
-12v (+5%, -3.0%)	18 mA (maximum)	11 mA (typical)

† As a general design objective, the junction temperature of all components on the DMV-177-XXX is limited to 110°C maximum (when the chassis cold-wall temperature is 85°C.) When reliability or performance factors permit, a component's junction temperature may exceed 110°C marginally.
SVME board operating temperature is based on air flow of 11 cfm.

The information in this document is subject to change without notice and should not be construed as a commitment by DY 4 Systems Inc. While reasonable precautions have been taken, DY 4 Systems Inc. assumes no responsibility for any errors that may appear in this document.
References to other documents of the exact issue, or if not shown, the issue in effect at the time of publication form a part of this specification to the extent referenced herein. In the event of a conflict, this specification will be considered a superseding requirement.

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