

LM215XB

FEATURES

- 480(W)×128(H) dot
- Recommendable controller LSI : HD61830
- Color tone : Yellow-green
- Viewing direction : 6 o'clock

MECHANICAL DATA (Nominal dimensions)

Module size270W×110H×11.5T(max.) mm
 Effective display area242W×69H mm
 Number of dots.....480W×128H dot
 Dot size0.43W×0.43H mm
 Dot pitch0.48W×0.48H mm
 Weight320 g

ABSOLUTE MAXIMUM RATINGS

| | min. | max. |
|--|------|------------|
| Power supply for logic ($V_{DD}-V_{SS}$) | 0 | 7.0 V |
| Power supply for LCD drive ($V_{DD}-V_{EE}$) | 0 | 19.0 V |
| Input voltage (V_i) (Note 1) | -0.3 | V_{DD} V |
| Operating temperature (T_a) | 0 | +40°C |
| Storage temperature (T_{stg}) | -20 | +60°C |

ELECTRICAL CHARACTERISTICS

$T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{ V}\pm 0.25\text{ V}$, $V_{EE}=-13.5\text{ V}\pm 0.5\text{ V}$

Input "high" voltage (V_{iH}) (Note 1)0.7 V_{DD} V min.

Input "low" voltage (V_{iL}) (Note 1)0.3 V_{DD} V max.

Clock frequency (f_{CL2})1.08 MHz min.

1.15 MHz typ.

1.23 MHz max.

Power supply current (I_{DD})6 mA typ.

(I_{EE})3 mA typ.

($D_1\sim D_4=\text{GND}$) ($f_{CL2}=1.15\text{ MHz}$) ($V_{DD}-V_O=14.5\text{ V}$)

Power supply for LCD drive (Recommended)

($V_{DD}-V_O$), Duty=1/64

$T_a=0^\circ\text{C}$ 15.5 V typ.

$T_a=25^\circ\text{C}$ 14.5 V typ.

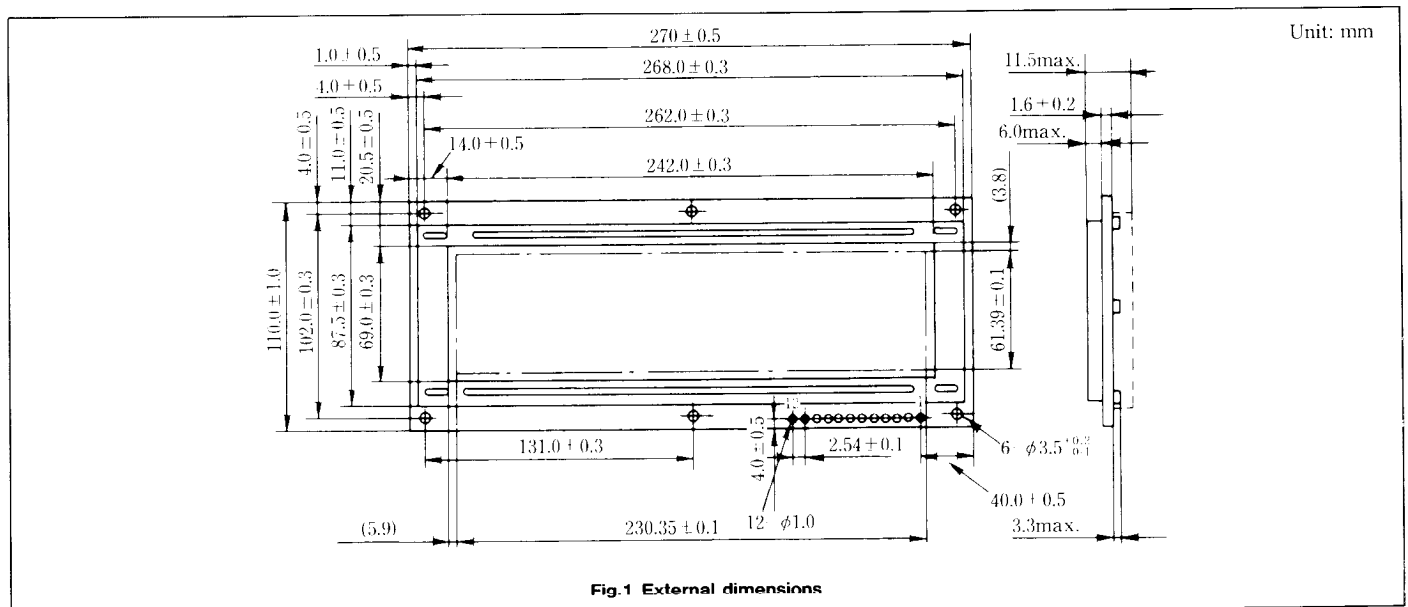
$T_a=40^\circ\text{C}$ 14.0 V typ.

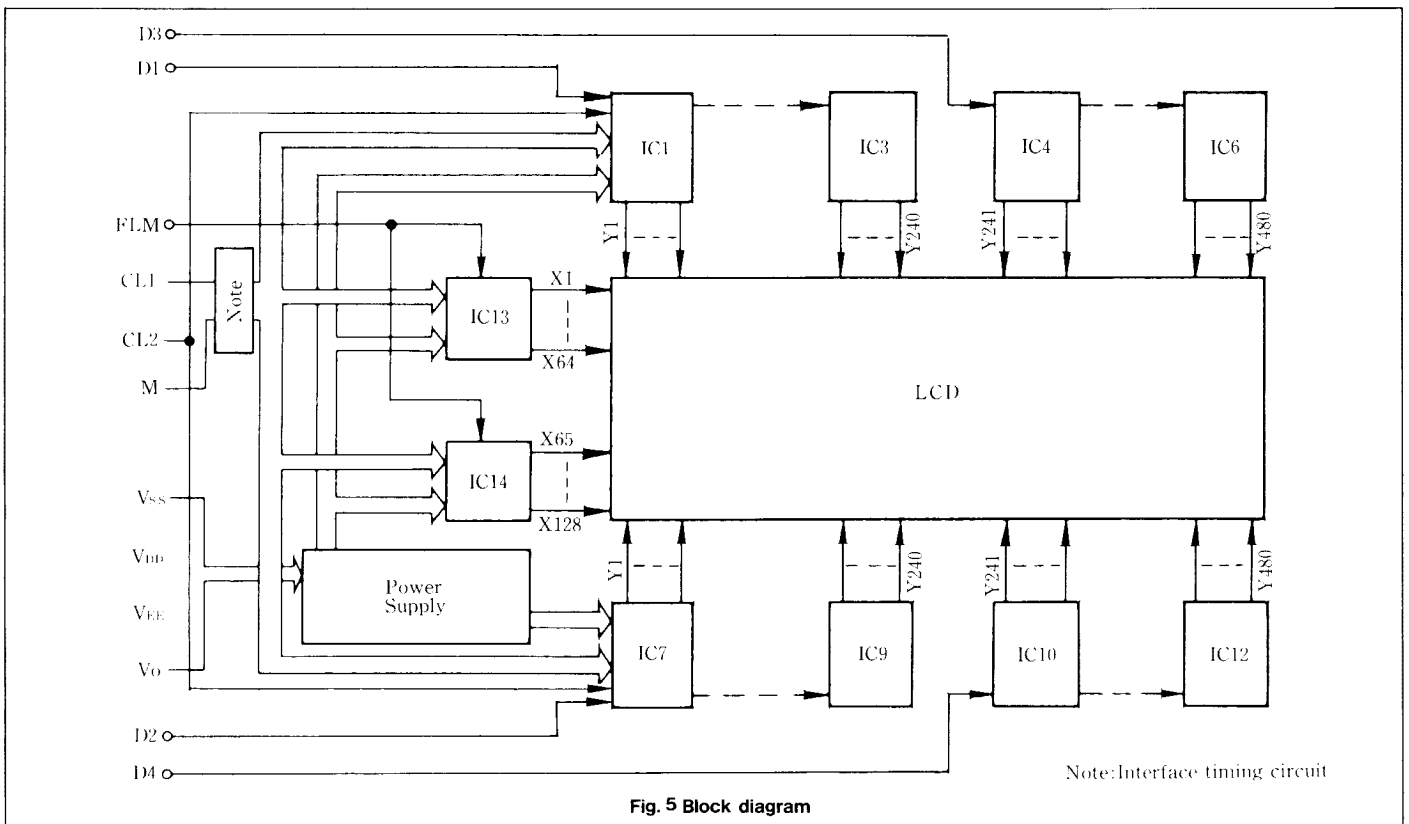
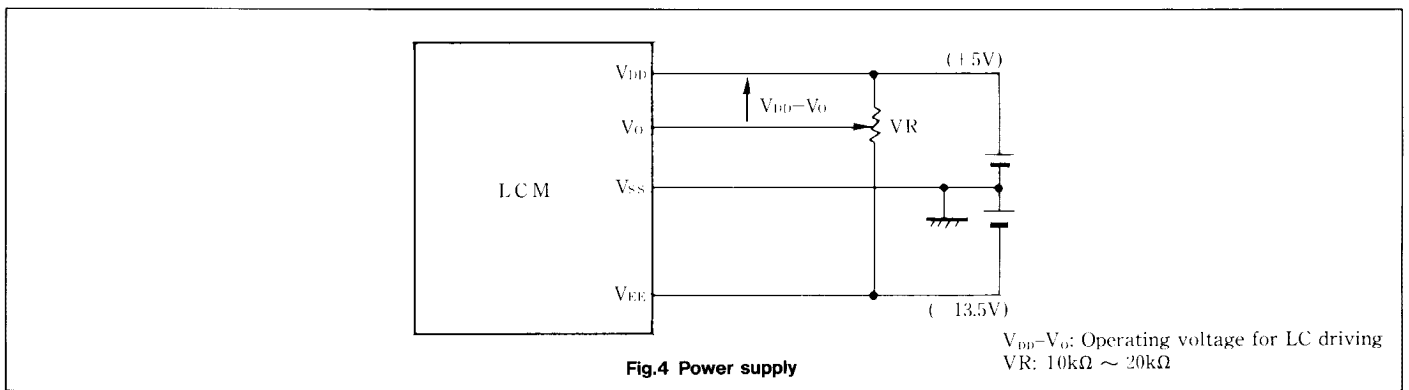
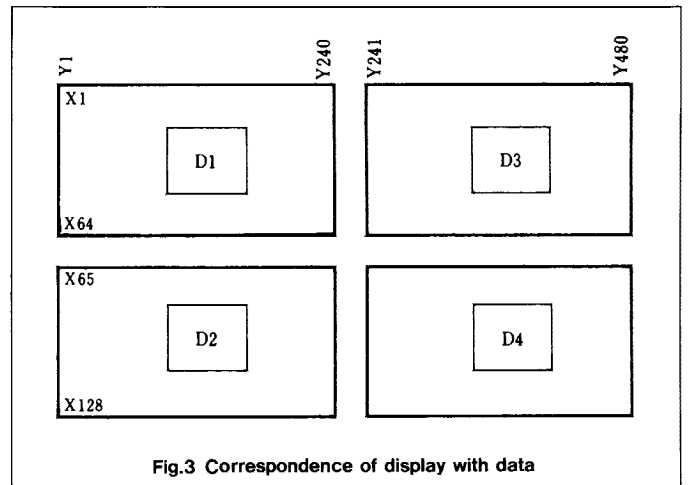
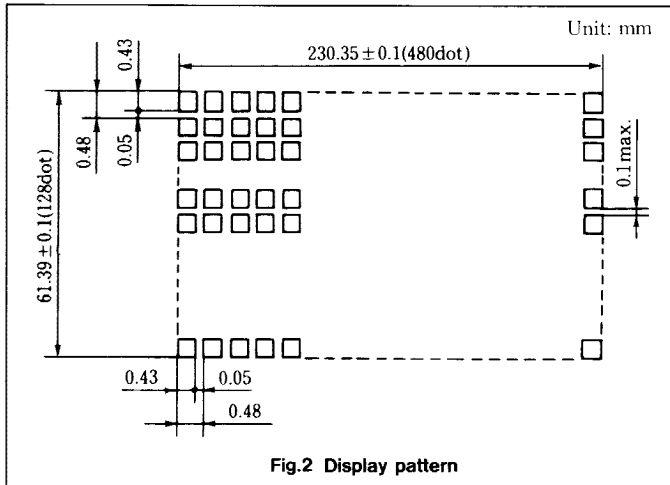
OPTICAL DATA See page 6

Note 1. Applied to CL1, CL2, D1~D4, M and FLM.

INTERNAL PIN CONNECTION

| Pin No. | Symbol | Level | Function |
|---------|-------------------------|-------|---|
| 1 | D1 | H/L | Serial row data (Upper left half) |
| 2 | D2 | H/L | Serial row data (Lower left half) |
| 3 | FLM | H | The FLM signal indicates the beginning of each display cycle. |
| 4 | M | H/L | Control signal for AC driving |
| 5 | CL1 | H→L | The CL1 latches the serial data in the shift registers. |
| 6 | CL2 | H→L | Clock signal for shifting the serial data |
| 7 | D3 | H/L | Serial row data (Upper left half) |
| 8 | D4 | H/L | Serial row data (Lower left half) |
| 9 | $V_{DD}(+5\text{V})$ | — | Power supply for logic circuit |
| 10 | $V_{SS}(\text{GND})$ | — | Ground |
| 11 | $V_{EE}(-13.5\text{V})$ | — | Power supply for LC driving |
| 12 | V_O | — | Operating voltage for LC driving |





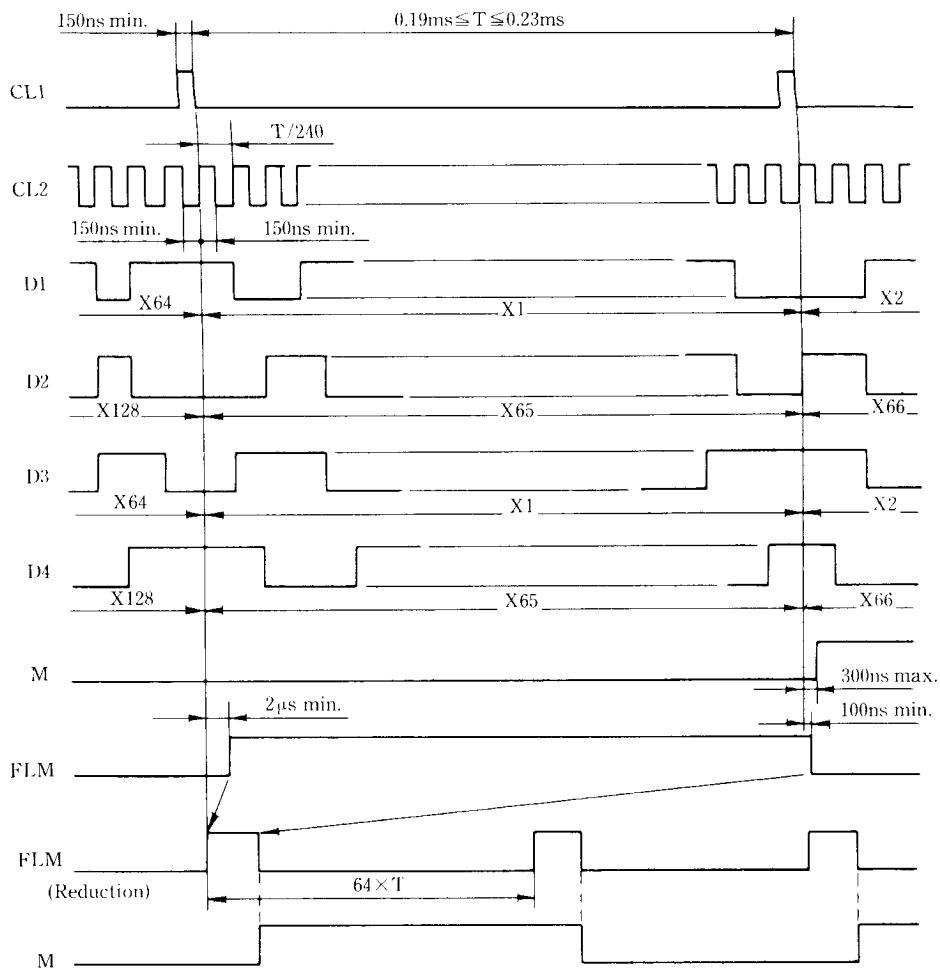


Fig.6 Interface timing

TIMING CHARACTERISTICS

| Item | Symbol | Min. | Typ. | Max. | Unit |
|----------------------|------------|------|------|------|------|
| CL2 cycle time | t_{CYC} | 810 | — | — | ns |
| CL2 pulse width (H) | t_{CWH} | 150 | — | — | ns |
| CL2 pulse width (L) | t_{CWL} | 150 | — | — | ns |
| CL1 set up time (1) | t_{SCL1} | 150 | — | — | ns |
| CL1 set up time (2) | t_{HCL1} | 150 | — | — | ns |
| Clock rise/fall time | t_r, t_f | — | — | 30 | ns |
| Data set up time | t_{DSU} | 100 | — | — | ns |
| Data hold time | t_{DH} | 100 | — | — | ns |
| CL1 delay time | t_{CL} | 150 | — | — | ns |
| "M" delay time | t_{CM} | — | — | 300 | ns |
| "FLM" set up time | t_{FS} | 100 | — | — | ns |
| "FLM" hold time | t_{FH} | 100 | — | — | ns |

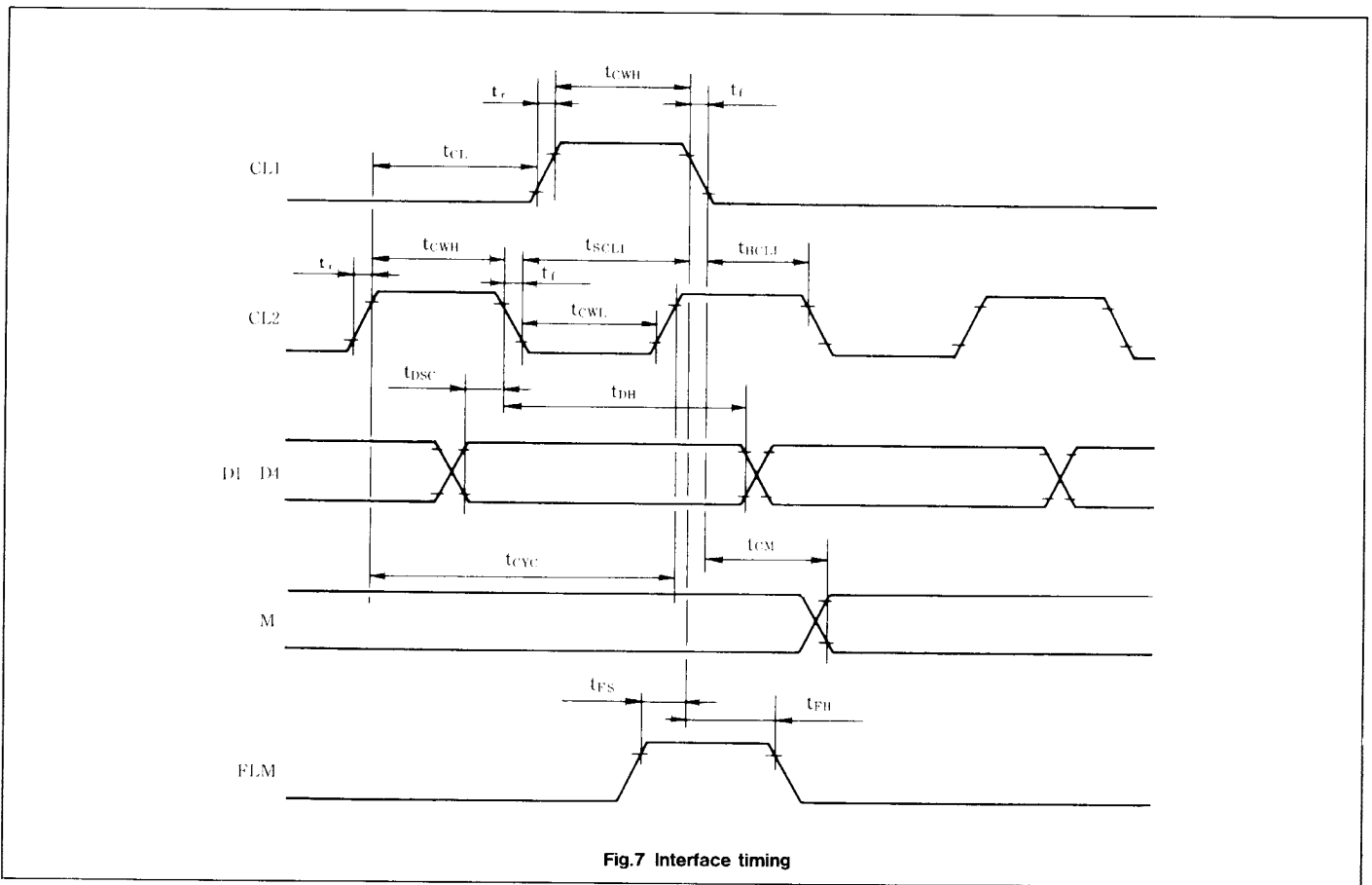


Fig.7 Interface timing