# SDC-19204/6 MONOBRID SERIES

## 10-, 12-, 14-, OR 16-BIT INDUSTRIAL SYNCHRO-TO-DIGITAL CONVERTERS

### DESCRIPTION

The SDC-19204/6 Monobrid Series converters are versatile state-of-the-art synchro-to-digital converters featuring programmable resolution and bandwidth, and velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and is available with accuracies up to 2 minutes +1 LSB. Resolution programming combines the high tracking rate of a 10-bit converter with the precision of a 16-bit device in one package.

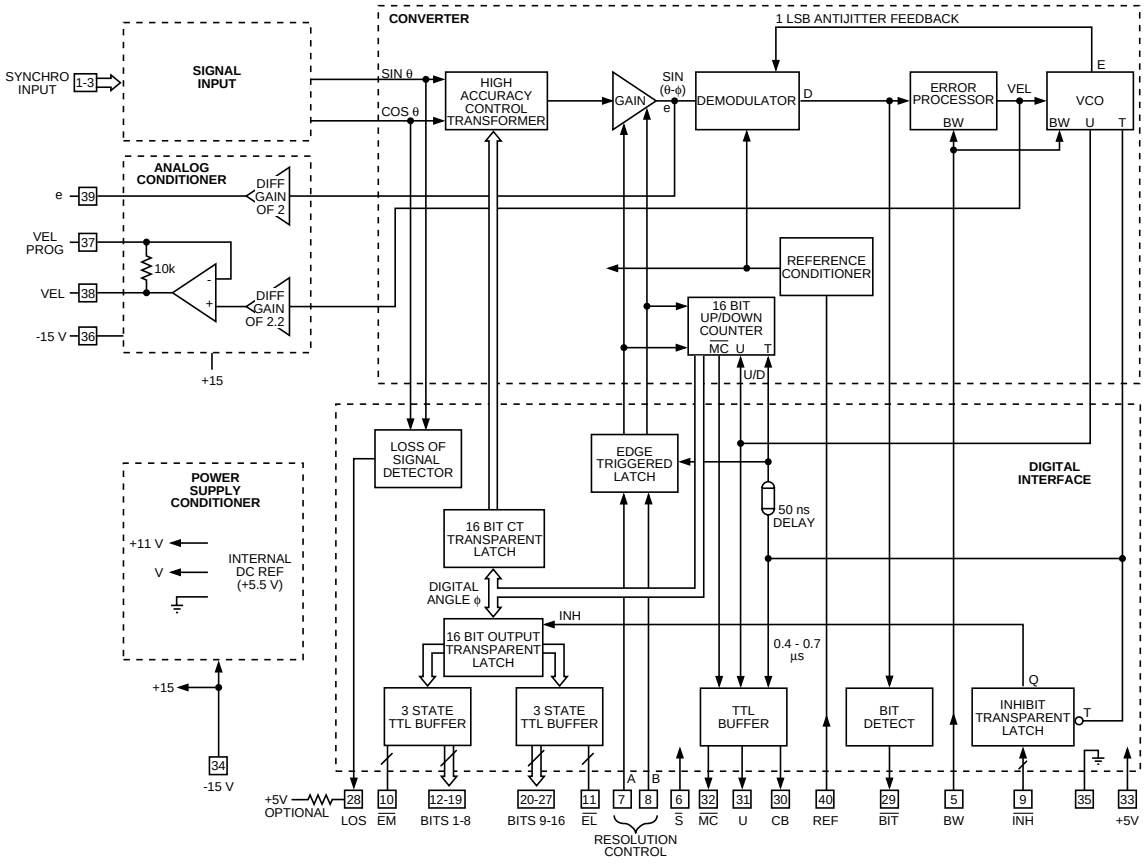
The velocity output (VEL) from the SDC-19204/6 is a ground-based voltage of 0 to ±10 VDC with a linearity of 2.0%. VEL may be scaled by a single external resistor to provide up to ±10 VDC for the required maximum tracking rate.

### APPLICATIONS

The SDC-19204/6 Series converters are designed for use in modern high-performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the SDC-19204/6 Series converters are ideal for motion control and position monitoring systems.

### *FEATURES*

- ***Low Cost***
- ***Ideal for Motor Control***
- ***Built-In-Test ($\overline{BIT}$) and Loss-Of-Signal (LOS) Outputs***
- ***Velocity Output Eliminates Tachometer***
- ***Programmable Resolution***
- ***Programmable Bandwidth***
- ***Accuracy to ±2.3 ARC Min.***




**SDC-19204/6 BLOCK DIAGRAM**

**TABLE 1. SDC-19204/6 SPECIFICATIONS**

These specifications apply over temperature range, power supply range and reference frequency amplitude range; ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

| PARAMETER | VALUE | DESCRIPTION |
|---|---|---|
| **RESOLUTION** | 10, 12, 14, or 16 bits | Programmable. |
| **ACCURACY GRADES** | 8, 4, 3, or 2 minutes | Max + 1 LSB of selected resolution (see Ordering Information). |
| **DIFFERENTIAL LINEARITY** | 16, 12, 8, or 4 | LSBs in the 16th bit (see Ordering Information). |
| **REPEATABILITY** | 1 LSB max | |
| **REF INPUT CHARACTERISTICS**<br>Voltage Range<br>Single-Ended Input Impedance<br>Frequency Range | <br>4-130 V rms<br>100k Ohm min; 110k Ohm nom<br>47 Hz to 1 kHz | <br><br><br>See TABLE 4., Dynamic Characteristics. |
| **SIGNAL INPUT CHARACTERISTICS**<br>Synchro<br>Zin Line to Line<br>Zin Each Line to Ground<br>Common Mode Range | <br>11.8 V L-L / 90 V L-L<br>52k Ohm / 123k Ohm<br>70k Ohm / 180k Ohm<br>25 V max / 180 V max | Voltage options and minimum input impedance balanced. |
| **DIGITAL INPUT/OUTPUT**<br>Logic Type<br>Inputs<br><br>Max Voltage w/o Damage<br>Loading<br>INH (Inhibit)<br>EM (Enable bits 1-8)<br>EL (Enable bits 9-16)<br>S (Control Transformer)<br>BW (Bandwidth)<br><br>Resolution Control<br>10 Bit<br>12 Bit<br>14 Bit<br>16 Bit | <br><br>Logic 0 = 0.8 V max<br>Logic 1 = 2.0 V min<br>-0.3 to 11 V<br>-10 µA max | <br>TTL/CMOS compatible.<br><br><br><br>Pull-up current source to + 5 V//5 pf max CMOS transient protected.<br>Logic 0 inhibits Logic 1 enables Data stable within 0.3 µs.<br>Logic 0 enables data valid within 150 ns Logic 1 high Z within 100 ns.<br>Logic 0 enables data valid within 150 ns Logic 1 high Z within 100 ns.<br>Logic 0 for Control Transformer, Logic 1 for normal tracking.<br>Logic 1 = High BW (53 Hz); Logic 0 = Low BW (13 Hz).<br><br>B (pin#8) A (pin#7)<br>0 0<br>0 1<br>1 0<br>1 1<br>Unused output bits are at logic 0. |
| **OUTPUTS**<br>Parallel Data<br>CB (Converter Busy)<br>U (Direction)<br>MC (Major Carry)<br>BIT (Built-in-Test)<br>LOS (Loss of Signal)<br>Drive Capability | <br>10, 12, 14, or 16 bits<br><br><br><br><br><br>Logic 0:1 TTL Load<br>Logic 1:10 TTL Loads<br>High Z:10 µA/5 pf max | <br>Natural binary angle positive logic.<br>0.4 µs to 0.7 µs positive pulse; leading edge initiates counter update.<br>Logic 1 counts up Logic 0 counts down.<br>Logic 0 at MC.<br>Logic 0 for BIT condition.<br>Logic 1 for LOS (1-3 µA pull-up to +5 V).<br>-1.6 mA at 0.4 V max.<br>0.4 mA at 2.8 V min. |
| **ANALOG OUTPUTS**<br>V (Internal DC ref)<br>VEL (Velocity)<br>e (AC error)<br><br><br><br>Dynamic Characteristics | <br>+5.5 V nom<br><br>50 mV rms per LSB of error<br>25 mV rms per LSB of error<br>12.5 mV rms per LSB of error<br>6.3 mV rms per LSB of error | <br><br>See TABLE 5 - Velocity Characteristics.<br>10-bit mode.<br>12-bit mode.<br>14-bit mode.<br>16-bit mode.<br>See TABLE 4 Dynamic Characteristics. |

| TABLE 1. SDC-19204/6 SPECIFICATIONS (CONTINUED) | | | | |
|---|---|---|---|---|
| **PARAMETER** | **VALUE** | | | **DESCRIPTION** |
| **POWER SUPPLY CHARACTERISTICS** | | | | |
| Nominal Voltage and Range | +15 VDC ±5% | +5 VDC ±10% | -15 VDC ±5% | Note: When analog outputs |
| Max Voltage w/o Damage | +18 V | +8 V | -18 V | are not required ground |
| Max Current | 25 mA | 10 mA | 15 mA | -15 V (pin 36). |
| **TEMPERATURE RANGES** | | | | |
| Operating | 0° C to +70° C | | | |
| Storage | -40° C to +120° C | | | |
| **PHYSICAL CHARACTERISTICS** | | | | |
| Size | 1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm) | | | 40-pin TDIP |
| Weight | 0.46 oz (13gm) | | | |

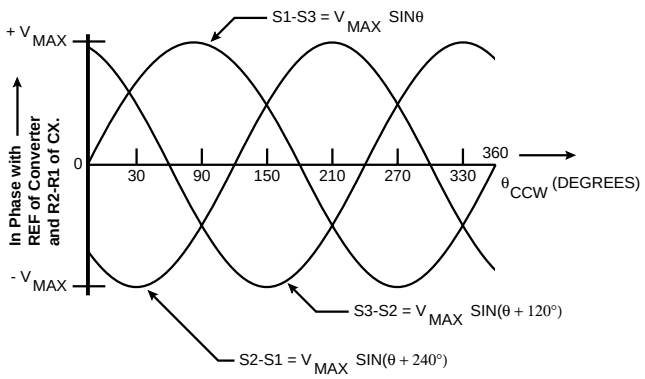
## INTRODUCTION

The SDC-19204/6 Series are small, 40-pin TDIP synchro-to-digital hybrid converters. As shown in the block diagram (FIGURE 1), the SDC-19204/6 can be broken down into five functional parts:

1. Signal Input Option
2. Converter
3. Analog Conditioner
4. Power Supply Conditioner
5. Digital Interface.

## SIGNAL INPUT

In a synchro, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta+120°)\cos\omega t$ and $\sin(\theta+240°)\cos\omega t$ are internally converted to resolver format; $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. FIGURE 2 illustrates synchro signals as a function of the angle $\theta$.




Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

**FIGURE 2. SYNCHRO SIGNALS**

## CONVERTER OPERATION

As shown in FIGURE 1, the converter section of the SDC-19204/6 contains a high accuracy control transformer, demodulator, error processor, voltage-controlled oscillator (VCO), up/down counter, zero-set timing, and reference conditioner. The converter produces a digital angle $\phi$ which tracks the analog input angle $\theta$ to within the specified accuracy of the converter.

The **control transformer** performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where :

$\theta$ is angle theta, representing the resolver shaft position.

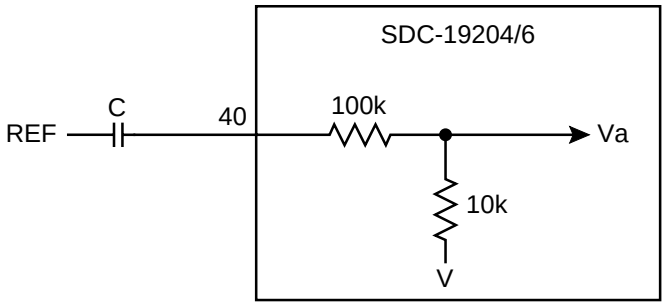
$\phi$ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting $\phi$ to make $(\theta - \phi) \rightarrow 0$, so that $\phi$ will repeat the shaft position $\theta$. The output of the **demodulator** is an analog DC level proportional to $\sin(\theta - \phi)$. The **error processor** receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal, which then drives the VCO. The VCO's clock pulses are accumulated by the **up/down counter**. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration, making the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The **reference conditioner** is a comparator that produces the square wave reference voltage which drives the demodulator. It is single-ended ground based with an input Z of 100k ohms min, 110k ohms nominal, resistive.

**MINIMIZING ERROR DUE TO QUADRATURE.** In those applications where highest accuracy is needed, the reference (REF) input can be phase-shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the synchro input. To determine the capacitor's value, see FIGURE 3.




Note: Choose C such that the $V_a$-to-REF phase lead is equal to the synchro-to-REF phase lead plus 9 µs.

**FIGURE 3. PHASE SHIFTING THE REF INPUT**

**QUADRATURE VOLTAGES.** In a synchro, quadrature voltages are, by definition, the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)
Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full-Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8 mV
Let: F.S. signal = 11.8 V
Let: a = 6°
Then: Magnitude of Error = 0.35 min ≈ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where :

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the synchro.
Carrier frequency is the REF in Hz.

## ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5 V to 0 V, provides a gain of 2 for AC Error (e) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VELOCITY PROGRAMMING section for more information.

## POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11 V from the +15 V supply. The +11 V will track the +15 V. Internal analog ground is one half of +11 V or +5.5 V, nom.

**INTERNAL DC REFERENCE VOLTAGE (V).** This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5 V and is proportional to the +15 VDC supply.

## DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command, allowing stable data to be read.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

By applying an Inhibit ($\overline{INH}$) command to the SDC-19204/6 the data will lock in the **output transparent latch** without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50 ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, pin 9) paragraph. The **BIT detect** circuitry monitors the error level (D) from the demodulator and the **LOS (loss of signal) detector** detects disconnected resolver inputs.

## LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10-bit resolution), bits 9-12 (12-bit resolution), bits 9-14 (14-bit resolution) or bits 9-16 (16-bit resolution). All unused LSBs will be at logic 0. TABLE 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ is activated with a logic 0, and are high impedance within 100 ns, max, after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5 V by -10 µA max current sources.

## DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5 V. The CB (Converter Busy) output is a positive, 0.4 to 0.7 µs pulse.

| TABLE 2 DIGITAL ANGLE OUTPUTS | | |
|---|---|---|
| **BIT** | **DEG/BIT** | **MIN/BIT** |
| 1 (MSB ALL MODES) | 180 | 10800 |
| 2 | 90 | 5400 |
| 3 | 45 | 2700 |
| 4 | 22.5 | 1350 |
| 5 | 11.25 | 675 |
| 6 | 5.625 | 387.5 |
| 7 | 2.813 | 168.5 |
| 8 | 1.405 | 84.38 |
| 9 | 0.7031 | 42.19 |
| 10 (LSB 10-BIT MODE) | 0.3516 | 21.09 |
| 11 | 0.1758 | 10.55 |
| 12 (LSB 12-BIT MODE) | 0.0879 | 5.27 |
| 13 | 0.0439 | 2.64 |
| 14 (LSB 14-BIT MODE) | 0.0220 | 1.32 |
| 15 | 0.0110 | 0.66 |
| 16 (LSB 16-BIT MODE) | 0.0055 | 0.33 |

Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in FIGURE 1). Data is valid 0.2 µs after the leading edge of CB (see FIGURE 4). The angle is determined by the sum of the bits at logic 1.

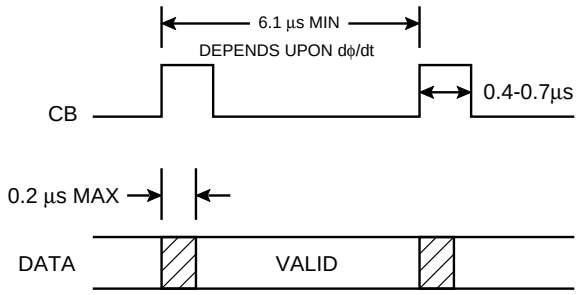



**FIGURE 4. CB TIMING**

## INHIBIT ($\overline{INH}$, PIN 9)

When an Inhibit ($\overline{INH}$) input is applied to the SDC-19204/6 the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see FIGURE 5). The output data bits are stable 0.3 µs after $\overline{INH}$ is driven to logic 0. A logic 0 at the T input of the Inhibit Transparent Latch latches the data; a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic 0 and the $\overline{INH}$ latch is transparent; when CB goes to logic 1, the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.3 µs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

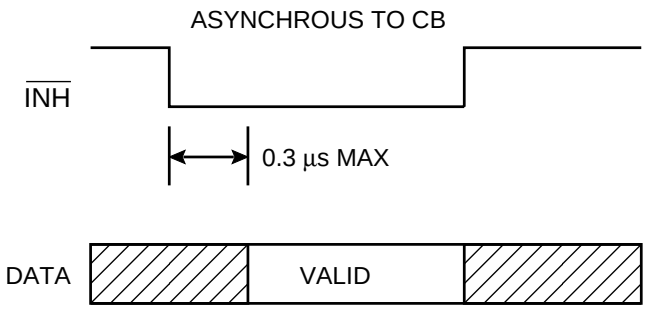



**FIGURE 5. INHIBIT TIMING**

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. FIGURE 6 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

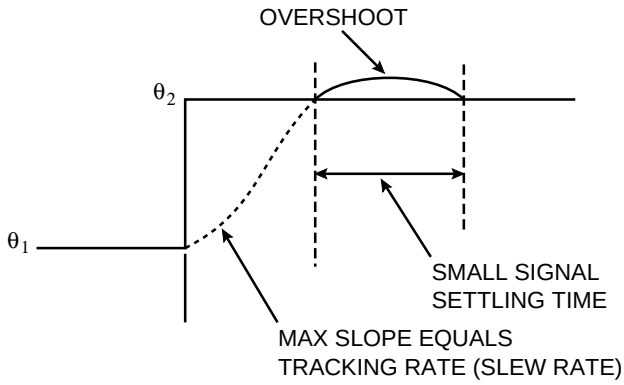



**FIGURE 6. RESPONSE TO A STEP INPUT**

## DATA TRANSFERS

Digital output data from the SDC-19204/6 can be transferred to 8-bit and 16-bit bus systems. For 8-bit systems, the MSB and LSB bytes are transferred sequentially (see FIGURES 7A and 7B). For 16-bit systems, all bits are transferred at the same time (see FIGURES 8A and 8B).

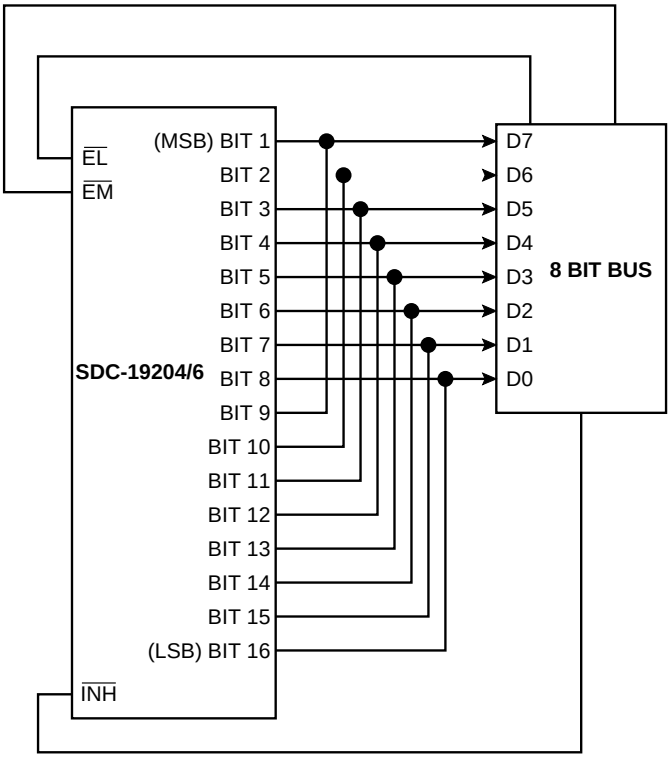



FIGURE 7A. 8-BIT BUS DATA TRANSFER

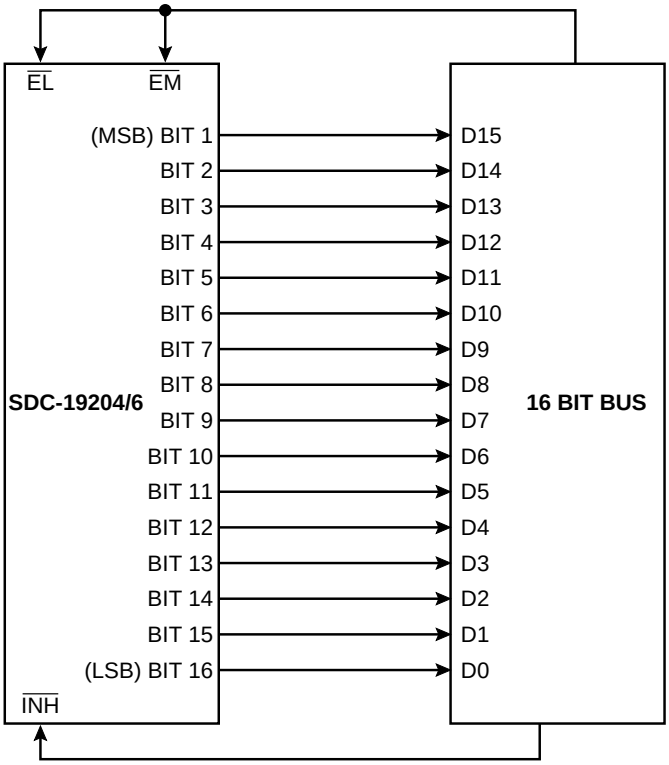



FIGURE 8A. 16-BIT BUS DATA TRANSFER

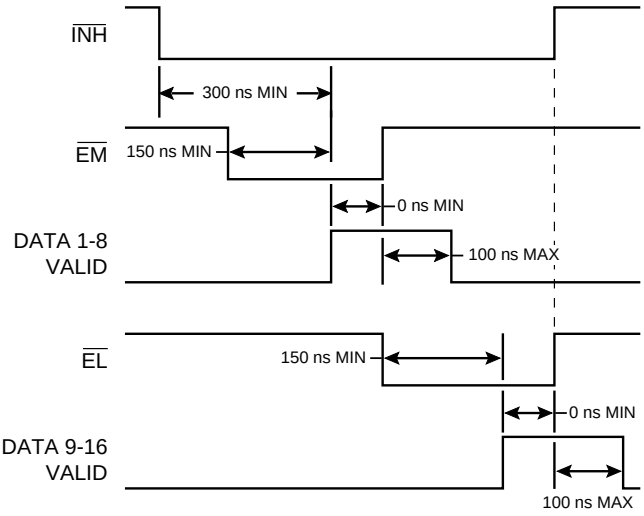



FIGURE 7B. 8-BIT BUS DATA TRANSFER TIMING

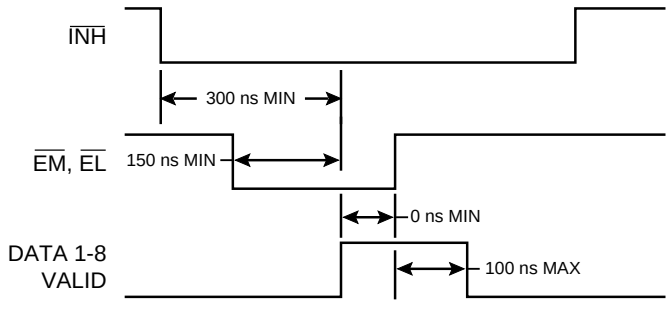



FIGURE 8B. 16-BIT BUS DATA TRANSFER TIMING

## PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see TABLE 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see FIGURE 9).

**TABLE 3. RESOLUTION CONTROL**

| B (PIN 8) | A (PIN 7) | RESOLUTION |
|---|---|---|
| 0 | 0 | 10 BIT |
| 0 | 1 | 12 BIT |
| 1 | 0 | 14 BIT |
| 1 | 1 | 16 BIT |

Note: All unused digital output data bits are at logic 0.

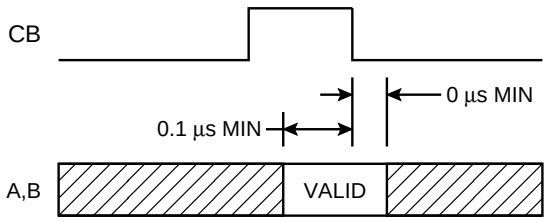



**FIGURE 9. RESOLUTION CONTROL TIMING**

## FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

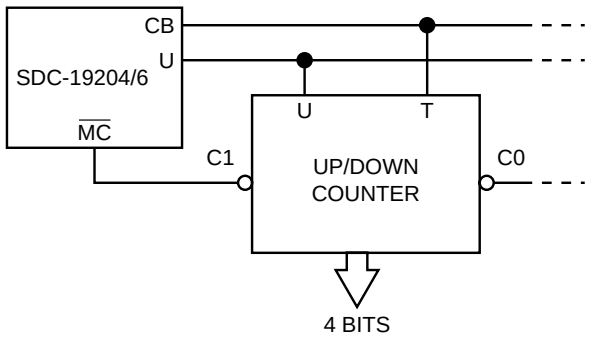
Since the SDC-19204/6 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the SDC-19204/6 for lower resolution, allowing the converter to settle faster for step inputs. High precision and fast settling can therefore be obtained simultaneously and automatically in one unit.

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

## MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multiturn applications. This signal is similar to a 4-bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See FIGURE 10 for a typical interconnection.

TURNS COUNTING




Notes:
(1) For the 4-bit up/down counter, use 74LS169B (TTL) or 4516 (CMOS).
(2) U = up/down line, logic 1 counts up.
(3) T = toggle line, counts on positive edge.

**FIGURE 10. TURNS COUNTING CONNECTION DIAGRAM**

## DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) timing is shown in FIGURE 11. It is at logic 1 to count up and logic 0 to count down. The logic level at (U) is valid at least 0.5 µs before and at least 20 ns after the leading edge of CB.

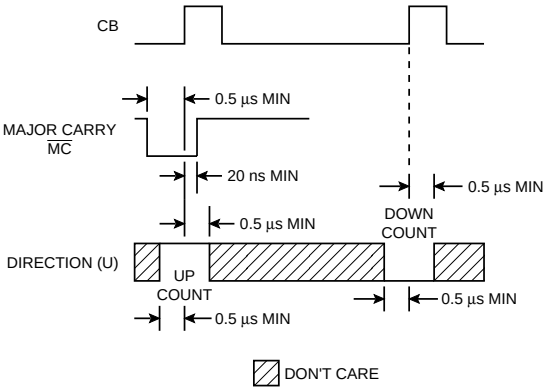



**FIGURE 11. DIRECTION OUTPUT (U) TIMING**

## SYSTEM SELF-TEST

The SDC-19204/6 provides two useful logic outputs for systems self test: $\overline{BIT}$ and LOS.

## BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test ($\overline{BIT}$) output monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the

converter loop cannot maintain input-output sync, or if the converter malfunctions where it cannot maintain the loop at a null.

## LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if all three synchro inputs are disconnected. With disconnected synchro inputs, unpredictable converter performance occurs.

## PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (13 Hz nominal), while a logic 1 selects high bandwidth (53 Hz nominal). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant ($K_a$) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\, A / \pi$$

$$K_a = A^2$$

**See Dynamic Characteristics TABLE 4 and FIGURES 15 to 17 for values.**

**TABLE 4. DYNAMIC CHARACTERISTICS**

| PARAMETER | UNITS | BANDWIDTH | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | HIGH | | | | LOW | | | |
| RESOLUTION | BITS | 10 | 12 | 14 | 16 | 10 | 12 | 14 | 16 |
| Input Frequency | kHz | .36-1 | * | * | * | .047-1 | * | * | * |
| Tracking Rate | RPS† | 160 | 40 | 10 | 2.5 | 40 | 10 | 2.5 | 0.62 |
| Bandwidth, CL | Hz | 53 | * | * | * | 13 | * | * | * |
| $K_a$ | 1/sec$^2$ | 14.4k | * | * | * | 3.6k | * | * | * |
| A1** | 1/sec | 0.4 | * | * | * | 0.1 | * | * | * |
| A2** | 1/sec | 36k | * | * | * | 9k | * | * | * |
| A** | 1/sec | 120 | * | * | * | 30 | * | * | * |
| B** | 1/sec | 60 | * | * | * | 15 | * | * | * |
| acc-1 LSB lag | °/sec$^2$ | 17k | 4.2k | 1.1k | 260 | 1.1k | 260 | 66 | 17 |
| Settling time max | msec | 110 | 110 | 200 | 500 | 550 | 600 | 1100 | 2400 |

†RPS minimum
*Same as value to left
**See FIGURE 15 for definitions of A1, A2, A, and B.

## CONTROL TRANSFORMER MODE (S, PIN 6)

The converter will function as a Control Transformer (CT) by placing S (pin 6) to logic 0. In the CT mode, the digital inputs are double buffered, EM is redefined as LM, EL is redefined as LL and $\overline{INH}$ becomes $\overline{LA}$ (see FIGURE 12). FIGURE 13 shows CT mode timing for a two-byte transfer.

The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the resolver input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.

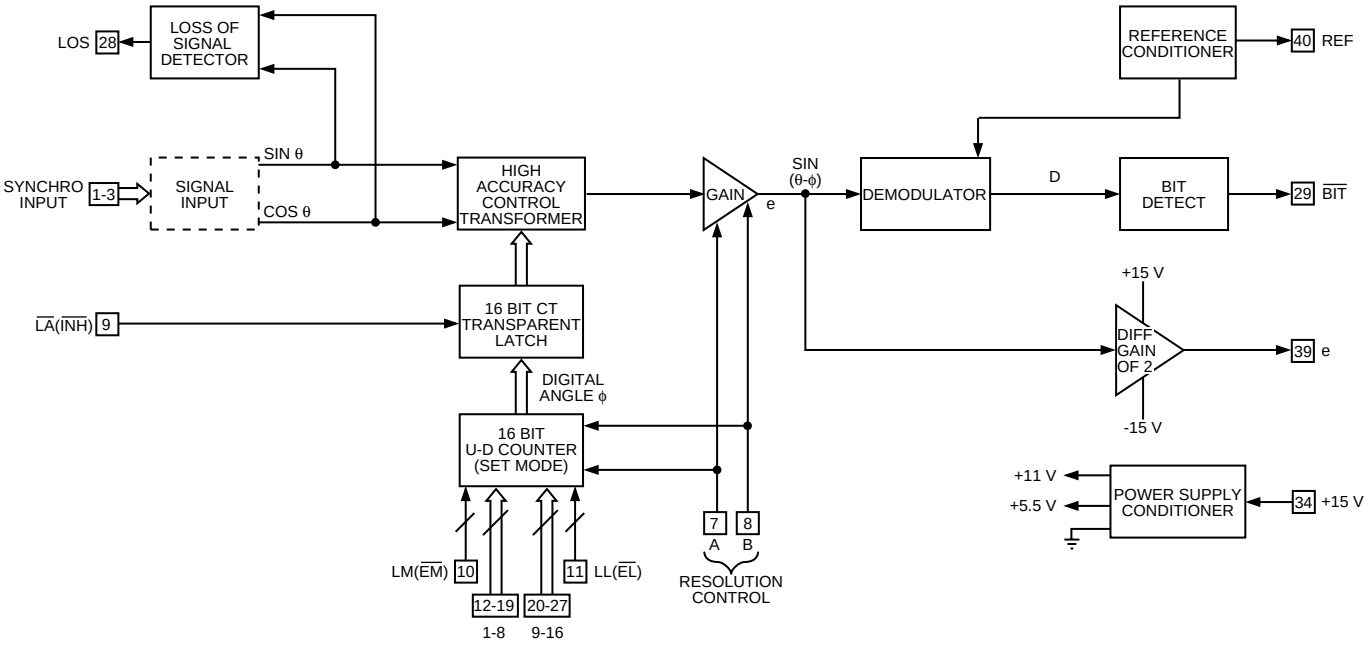
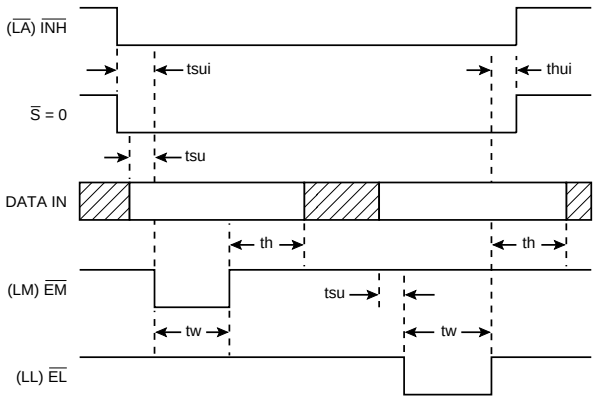



**FIGURE 12. CONTROL TRANSFORMER BLOCK DIAGRAM**




Notes:
(1) tw = 100 ns min (pulse width)
th = 50 ns min (hold time)
thui = 0 ns min (hold time inhibit)
tsu = 0 ns min (setup time)
tsui = 300 ns min (setup inhibit)
(2) When S is low:
(LM) EM is latch control for MSB byte,
(LL) EL is latch control for LSB byte,
1 - data held in latch,
0 - latch is transparent,
(3) (LA) INH is latch control for CT latch:
1 - latch is transparent,
0 - data held in latch.

**FIGURE 13. CT MODE TIMING - TWO-BYTE TRANSFER, DOUBLE BUFFERED**

## ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground -15 V (pin 36).

## AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle $\theta$ and the digital input angle $\phi$, $(\theta - \phi)$, with a scaling of:

50 mVrms/LSB (10-bit mode)
25 mVrms/LSB (12-bit mode)
12.5 mVrms/LSB (14-bit mode)
6.3 mVrms/LSB (16-bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference. The e output can swing ±10 V peak min with respect to ground when the voltage level of the ±15 V power supplies are 15 V. The output level range changes proportionally with the power supply level.

## VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage-controlled oscillator (VCO), as shown in FIGURE 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO. The maximum VEL output can swing ±10 V min with respect to ground when the voltage level of the ±15 V power supplies are 15 V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in TABLE 5. The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

**TABLE 5. VELOCITY OUTPUT CHARACTERISTICS**

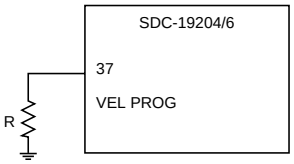
| PARAMETER | UNIT | SDC-19204/6 | |
|---|---|---|---|
| | | TYP | MAX |
| Polarity | | (positive for increasing angle) | |
| Voltage scaling | RPS/V | See Voltage Scaling TABLE 6. | |
| Scale Factor | % | 10 | 15 |
| Scale Factor TC | PPM/°C | 100 | 200 |
| Reversal Error | % | 1 | 2 |
| Linearity | % output | 1 | 2 |
| Zero Offset | mV | 15 | 40 |
| Zero Offset TC | µV/°C | 25 | 50 |
| Load | k Ohms | - | 3 |
| Output Voltage | V | ±13 | ±10 min |

## VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG (pin 37) to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

$$R = \frac{10 \quad B/A}{1 - B/A}$$

Where:
R = external resistor in k Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)




To determine A, refer to TABLE 6, Voltage Scaling.

**TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)**

| BW | 10 BIT | 12 BIT | 14 BIT | 16 BIT |
|---|---|---|---|---|
| HIGH | 16 | 4 | 1 | 0.25 |
| LOW | 4 | 1 | 0.25 | 0.062 |

## DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-19204/6 superior dynamic performance as listed in TABLE 4.

## VELOCITY RESPONSE

A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. The VEL filter is shown in FIGURE 14.

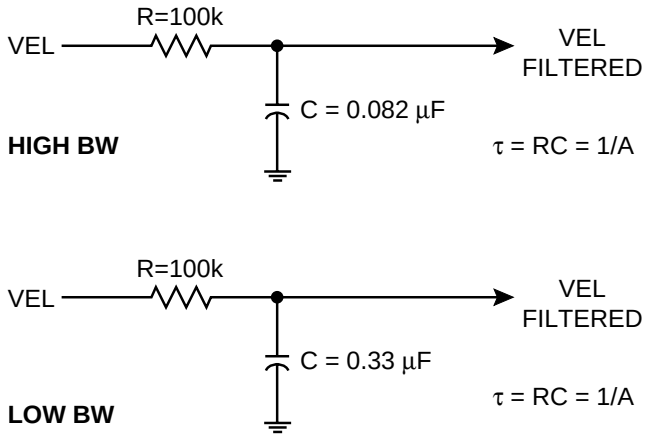


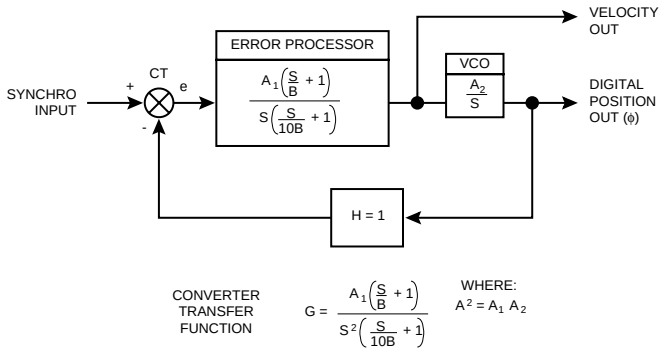

**FIGURE 14. VEL OUTPUT FILTER**

## TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (FIGURE 15) and open and closed-loop Bode plots (FIGURES 16 and 17 and TABLE 4 lists the parameters relating to the SDC-19204/6's dynamic characteristics for different resolution and bandwidth modes.

## ACCURACY AND RESOLUTION

TABLE 7 lists the total accuracy including quantization for the various resolution and accuracy grades.




Note: See TABLE 4 for values of A1 A2, and B

**FIGURE 15. TRANSFER FUNCTION BLOCK DIAGRAM**

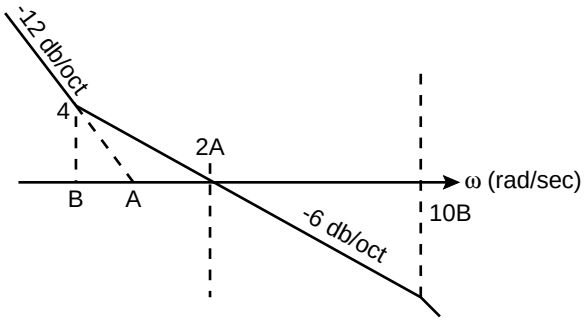



**FIGURE 16. OPEN LOOP BODE PLOT**

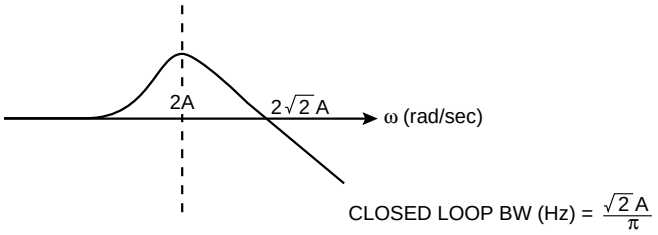



**FIGURE 17. CLOSED LOOP BODE PLOT**

**TABLE 7. ACCURACY/RESOLUTION**

| SDC-1920X SERIES MODEL NO. | ACCURACY | 10 BIT | 12 BIT | 14 BIT | 16 BIT |
|---|---|---|---|---|---|
| SDC-1920X-304 | 2' + 1 LSB | 23.1 | 7.3 | 3.3 | 2.3 |
| SDC-1920X-303 | 3' + 1 LSB | 24.1 | 8.3 | 4.3 | 3.3 |
| SDC-1920X-302 | 4' + 1 LSB | 25.1 | 9.3 | 5.3 | 4.3 |
| SDC-1920X-301 | 8' + 1 LSB | 29.1 | 13.3 | 9.3 | 8.3 |

## SDC-19204 APPLICATIONS

### *USING THE SDC-19204/6 IN THE CT MODE*

The CT mode can be applied in servo systems, as shown in FIGURE 18. In this application changes in position are commanded by the computer through signals fed to the CT. The CT then drives the motors through DC power amplifiers.

### *MULTITURN APPLICATIONS-USE OF MAJOR CARRY ($\overline{MC}$, PIN 32)*

Refer to Major Carry paragraph for details.

### *USING THE SDC-19204/6 AS AN S/D WITH VEL TO STABILIZE POSITION LOOP*

FIGURE 19 illustrates a typical use of a SDC-19204/6 connected as an S/D using the VEL output to stabilize the position loop.

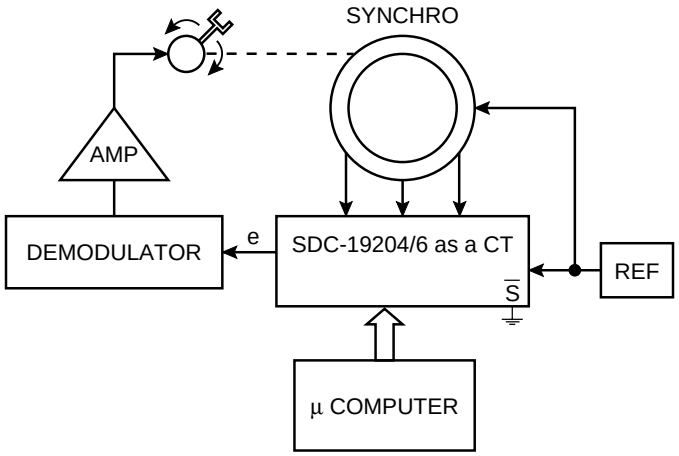



**FIGURE 18. CT MODE APPLICATION**

### *INTERFACING THE SDC-19204/6 WITH AN IBM PC/XT/AT®*

The SDC-19204/6 can be connected to an IBM PC/XT/AT through the IBM PC Bus located at address HEX 300 through 303. This location is reserved by the PC for prototype cards. FIGURE 21 illustrates the connection to the IBM PC Bus; FIGURE 20 illustrates the timing considerations for the interface.

### SDC-19204/6-To-IBM PC/XT/AT Theory of Operation

1. The port address where the SDC-19204/6 is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the SDC-19204/6 to be placed on the Bus. When A1 is high, bits 1-8 are selected.

3. Address line A0 sets and resets the SDC-19204/6 INHIBIT ($\overline{INH}$) line. When A0 is low, the INHIBIT command is invoked.

4. To read the output of the SDC-19204/6 perform the following:

   a. Send address HEX 302 to INHIBIT the SDC-19204/6 (hold data stable) and place bits 1-8 on the Bus. Read and store data on D0 to D7.

   b. Send address 300 HEX to keep the SDC-19204/6 in the INHIBIT mode and place bits 9-14 on the Bus. Read and store data on D0 to D7.

   c. Read address 301 HEX or 303 HEX to release the SDC-19204/6 from the INHIBIT mode and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5µs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus reads on the next negative clock edge.

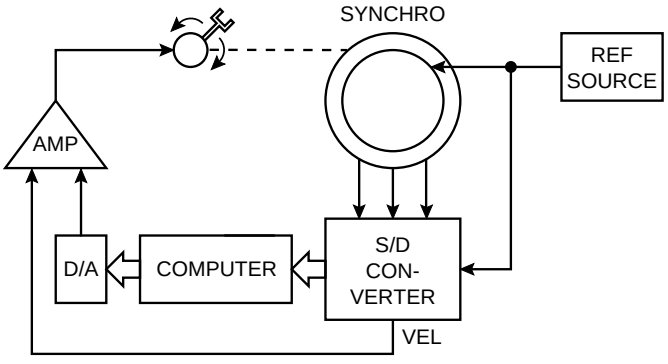



**FIGURE 19. S/D WITH VEL TO STABILIZE POSITION**

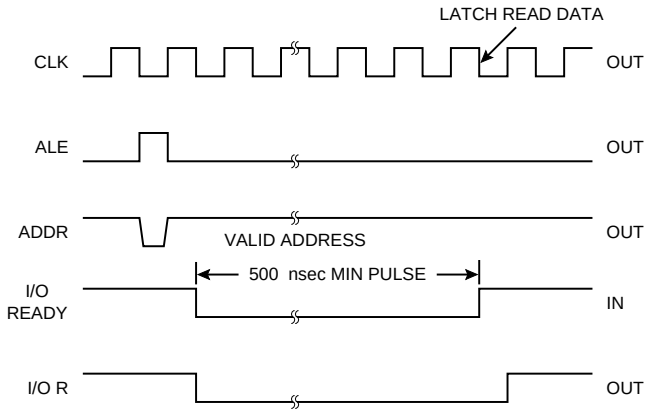



**FIGURE 20. PC APPLICATION - I/O READ CYCLE TIMING**

®IBM PC/XT/AT is a registered trademark of International Business Machines Corporation.

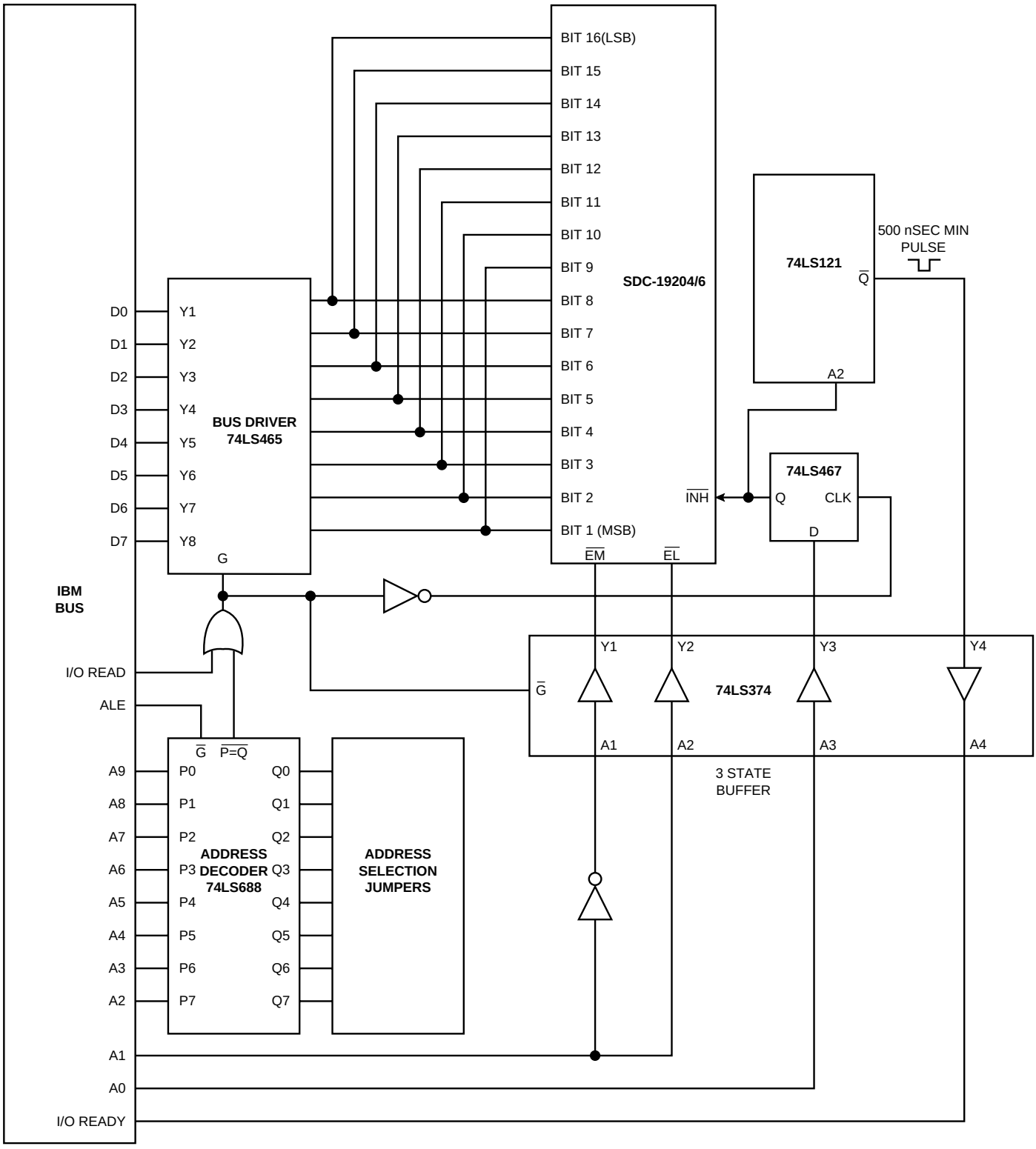



FIGURE 21. SDC-19204/6-TO-PC CONNECTION DIAGRAM

| TABLE 8. SDC-19204/6 PIN FUNCTIONS | | | |
|---|---|---|---|
| **PIN NO.** | **TITLE** | **I/0** | **FUNCTION** |
| 1 | S1 | I | Synchro Input. |
| 2 | S2 | I | Synchro Input. |
| 3 | S3 | I | Synchro Input. |
| 4 | NC | I | No connection. |
| 5 | BW | I | Bandwidth. Logic 1 for high BW (53 Hz); logic 0 for low BW (13 Hz). |
| 6 | S | I | Control Transformer Set. Logic 1 for normal tracking logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input and for presetting the converter to a specific angle to reduce the step response time. |
| 7 | A | I | Resolution Control A. Change Resolution to 10, 12, 14, or 16 bit depending on logic level (See TABLE 3). |
| 8 | B | I | Resolution Control B. Change Resolution to 10, 12, 14, or 16 bit depending on logic level (See TABLE 3). |
| 9 | $\overline{INH}$ | I | Inhibit. Logic 0 prevents digital output bits from changing. |
| 10 | $\overline{EM}$ | I | Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits. |
| 11 | $\overline{EL}$ | I | Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits. |
| 12 | 1 | O | Digital Output Bit 1 (MSB all modes). |
| 13 | 2 | O | Digital Output Bit 2. |
| 14 | 3 | O | Digital Output Bit 3. |
| 15 | 4 | O | Digital Output Bit 4. |
| 16 | 5 | O | Digital Output Bit 5. |
| 17 | 6 | O | Digital Output Bit 6. |
| 18 | 7 | O | Digital Output Bit 7. |
| 19 | 8 | O | Digital Output Bit 8. |
| 20 | 9 | O | Digital Output Bit 9. |
| 21 | 10 | O | Digital Output Bit 10 (LSB-10 BIT MODE). |
| 22 | 11 | O | Digital Output Bit 11. |
| 23 | 12 | O | Digital Output Bit 12 (LSB-12 BIT MODE). |
| 24 | 13 | O | Digital Output Bit 13. |
| 25 | 14 | O | Digital Output Bit 14 (LSB-14 BIT MODE). |
| 26 | 15 | O | Digital Output Bit 15. |
| 27 | 16 | O | Digital Output Bit 16 (LSB-16 BIT MODE). |
| 28 | LOS | O | Loss of signal. Used for system safety; the LOS output changes from logic 0 to 1 if all three synchro inputs are disconnected. |
| 29 | $\overline{BIT}$ | O | Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds approximately 65 bits . Also logic 0 for an over-velocity condition. |
| 30 | CB | O | Converter Busy. Indicates digital output update. |
| 31 | U | O | Direction. Logic 1 to count up; logic 0 to count down. |
| 32 | $\overline{MC}$ | O | Major Carry. Used for turns counting applications; normally high goes low for all 1 ‘s when counting up or all 0’s when counting down. |
| 33 | +5 V | I | Supply Voltage. |
| 34 | +15 V | I | Supply Voltage. |
| 35 | GND | - | Ground. |
| 36 | -15 V | I | Supply Voltage. |
| 37 | VEL PROG | I | Velocity Programming. Increase output scale factor with external resistor (R) from VEL PROG (pin 37) to ground. |
| 38 | VEL | O | Velocity. DC voltage proportional to angular velocity. |
| 39 | e | O | AC Error. Used in CT mode; e is proportional to the difference between the resolver input angle $\theta$ and the digital output angle $\phi$ ($\theta$ - $\phi$). |
| 40 | REF | I | AC Reference Input. Used to drive internal demodulator. |

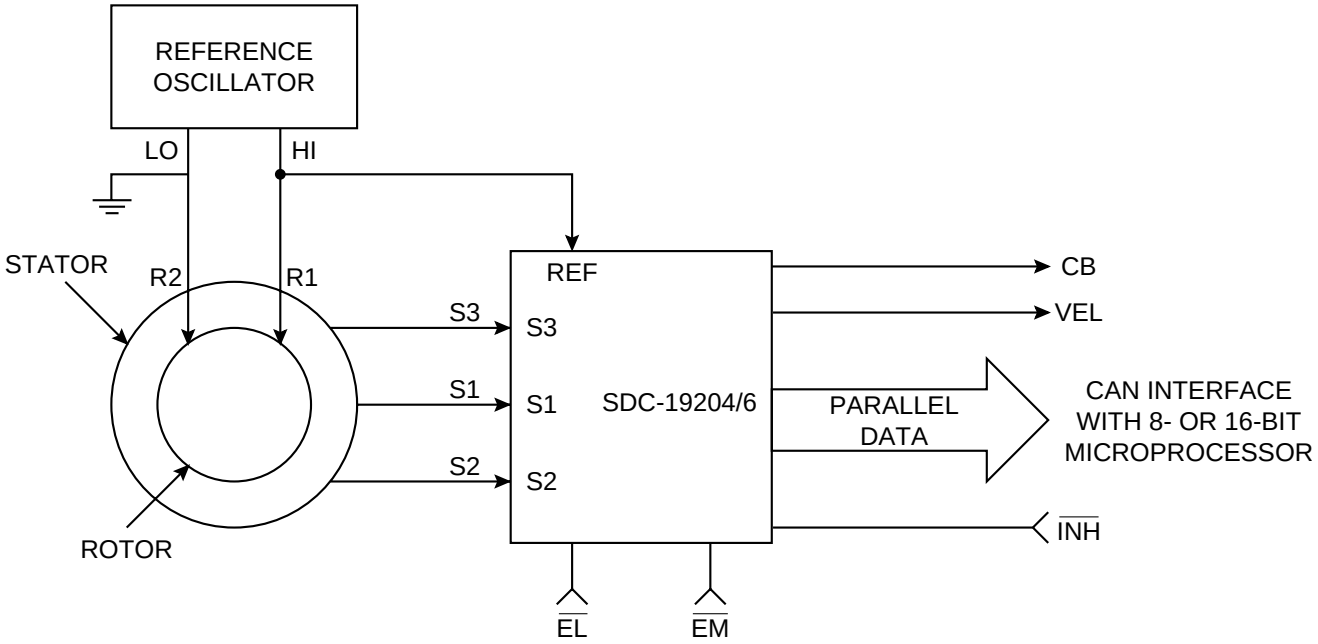



**FIGURE 22. SYNCHRO CONNECTION**

## SOURCES OF SOCKETS FOR THE SDC-19204/6

The following companies are sources of sockets for use with the SDC-19204/6 Series. Consult them for more information.

**Aries Electronics, Inc.**
**P.O. Box 130**
**Trenton Avenue**
**Frenchtown, NJ 08825-0130**
**Tel: 1-908-996-6841**
**http://www.arieselec.com**

Single In-Line Socket
Strip-Line Socket

Part No.20-05511 -11

**Circuit Assembly Corp.**
**18 Thomas Street**
**Irvine, CA 92618-2777**
**Tel: 714-855-7887**
**http://www.ca-online.com**

Part No. CA-20-STL-XX XX-X

## CONNECTING THE SDC-19204/6

The SDC-19204/6 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

**Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F). Since the SDC-19204/6 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.**

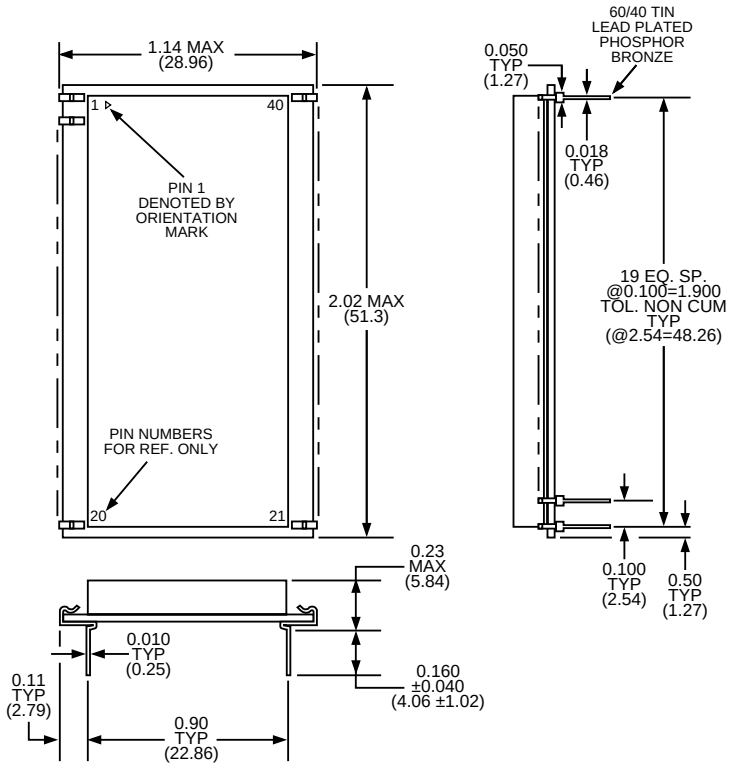



**FIGURE 23. SDC-19204/6 MECHANICAL OUTLINE**

## ORDERING INFORMATION

SDC-1920X-30X

**Accuracy:**
- 1 = 8 min + 1 LSB (12 LSBs Differential Linearity)
- 2 = 4 min +1 LSB (8 LSBs Differential Linearity)
- 3 = 3 min +1 LSB (4 LSBs Differential Linearity)
- 4 = 2 min +1 LSB (4 LSBs Differential Linearity)

**Configuration:**
- 4 = 11.8 V, 2% Linearity
- 6 = 90 V, 2% Linearity

Note: Differential Linearity is x LSB in the 16th bit.

105 Wilbur Place, Bohemia, New York 11716-2482

**For Technical Support - 1-800-DDC-5757 ext. 7389 or 7413**

**Headquarters -** Tel: (631) 567-5600 ext. 7389 or 7413, Fax: (631) 567-7358
**Southeast -** Tel: (703) 450-7900, Fax: (703) 450-6610
**West Coast -** Tel: (714) 895-9777, Fax: (714) 895-4988
**Europe -** Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
**Asia/Pacific -** Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689
**World Wide Web -** http://www.ddc-web.com

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